Syed Tahir Hussain Rizvi

Address: Corso Monte Grappa 94, Torino, Italy E-Mail: tahir_rizvi@outlook.com, syed.rizvi@polito.it Mobile: +39-3473694140, Skype ID: tahir_rizvi Date of Birth: 16-12-1986

OBJECTIVES

To work in a challenging environment where the chances of learning are high. Looking for challenging opportunities, which utilize my educational background and experience.

ACADEMIC QUALIFICATION

- PhD. Computer and Control Engineering (Funded by Telecom Italia) 2014-2018 Politecnico di Torino, Torino, Italy Quality Award 2016 for PhD activities
- M.Sc. Computer Engineering 2009-2013 CGPA: 3.71

University of Engineering and Technology, Lahore, Pakistan

 B.Sc. Electrical Engineering 2004-2008 CGPA: 3.86

University of Central Punjab, Lahore, Pakistan

WORK EXPERIENCE

- Postdoctoral Researcher in Department of Electronics and Telecommunications (Feb 2021 - Present)
 Politecnico di Torino, Torino, Italy Funded by Telecom Italia
- Assistant Professor in Department of Computer Engineering (June 2018 - Jan 2021) The University of Lahore, Lahore, Pakistan
- Visiting Researcher in Department of Control and Computer Engineering (DAUIN) (Jan 2018 - May 2018)
 Politecnico di Torino, Torino, Italy
- Assistant Professor in Faculty of Engineering (FOE) (Oct 2008 - Aug 2014) University of Central Punjab, Lahore, Pakistan
 - Main Subjects Taught at Graduate and Undergraduate Level:
 - Advanced Embedded System Design:
 - Software Taught: Atmel Studio for ATMega328P, Proteus for Embedded System Simulation and Debugging.
 - > Language Taught: Assembly & C/C++ Language.
 - Micro-Processor/Micro-Controller Based Embedded Systems:
 - Software Taught: Keil Compiler for Atmel-8051 Family, Proteus for Embedded System Simulation and Debugging.
 - > Language Taught: Assembly & C/C++ Language.
 - > Hardware Kit: Atmel-8051 Microcontroller Kit, 8086/8088 Architecture Based Kit.

- ✤ Digital System Design (FPGA): "Advanced form of Digital Logic Design".
 - Software Taught: EDA Tool for HDL (Xilinx ISE, Vivado Design Suite).
 - > Language Taught: Hardware Description Language (VHDL).
 - > Hardware Kit: Spartan-3 FPGA Kit.

Computer Communications and Networks:

- Software Taught: Packet Tracer, WireShark, VMware Workstation.
- > Hardware: Cisco Routers and Switches.

***** Other Miscellaneous Subjects & Softwares Taught:

Digital Image Processing, MATLab.

Projects Supervised:

- IOT-based Monitoring and Control of Farming System
- > Control of Prosthetic Hand through EEG Headset
- > Wireless Shadow Dexterous Hand for Hazardous Environment
- > Monitoring of Processing Unit using Wireless Sensor Network
- Visual Impairment AID using Haptic and Sound Feedback
- > Microcontroller based GAS Leakage Detection, Control and Alert
- I-Button and Voice Recognition Based Security Lock

> Small Projects

 Cell Phone Controlled Home Appliances, Voice Controlled Wheelchair, GSM based Security System, Metering of Different Parameters using Microcontroller

✤ Coordinator of MS Program and Quality Enhancement Cell (2018- 2021) in UOL

- Managed all relevant information for MS students about the offered Courses including thesis procedures and degree requirements as MS Program Coordinator
- Produced and managed all relevant information for accreditation of MS program from relevant body as Quality Enhancement Cell Coordinator

Graduate Student Coordinator (2012- 2014) in UCP

Produced all relevant information for students about the offered Courses including timetable, assessment procedures and degree requirements

***** Technical Team Member in National Education Campaign (RoboSprint 2013)

- > Designed Course Material and Lab Sessions to be conducted in Workshops
 - Conducted Workshops across the Country at Participating Institutes

RESEARCH WORK

• PhD Thesis related to Deep Neural Network on Embedded Systems:

Visual Analysis Algorithms for Embedded Systems

A framework is designed and developed to deploy the deep classifiers on the embedded platforms for real-time Visual analysis. The CUDA computing framework is used for the realization of identical neural architectures on embedded devices to exploit the already trained networks. Intermediate frameworks and memory consuming computational packages are avoided using the proposed CUDA-only scheme to resolve the problem of software dependencies and reduce the storage requirements. Proposed framework is optimized to improve the inference performance, storage requirements and energy efficiency. Proposed optimized framework can be utilized to realize the neural network based real-time classification problems on the embedded GPUs.

Master Thesis related to Parallel Control of Machines in Field of Embedded Systems: An Inverse Kinematics Algorithm-Based Parallel Control of Welding Arm

Motion control system of jointed robotic arm is implemented using parallel processing. Inverse kinematics Algorithm is selected to control robotic arm. This algorithm is designed in VHDL and physically implemented on FPGA Kit. By using Parallelism of VHDL and FPGA, inverse kinematics algorithm is executed at much faster speed than other controllers having pipelined architecture. Thus, execution time is reduced from milli-seconds to nano-seconds.

BRIEF LIST OF PUBLICATIONS

- A Gentle Introduction to Reinforcement Learning and its Application in Different Fields (IEEE Access, Vol 8, 2020), SCIE Indexed
- On Hiding Secret Information in Medium Frequency DCT Components Using Least Significant Bits Steganography

(Computer Modeling in Engineering & Sciences, 118(3), 2019), SCIE Indexed

 Rice Grain Identification and Quality Analysis using Image Processing based on Principal Component Analysis

(In International Symposium on Recent Advances in Electrical Engineering, Oct 2018, Pakistan)

 Increasing Distance Increasing Bits Substitution (IDIBS) Algorithm for Implementation of VTVB Steganography

(Computer Modeling in Engineering & Sciences, 117(1), 2018), SCIE Indexed

 Deep Classifiers-Based License Plate Detection, Localization and Recognition on GPU-Powered Mobile Platform

(Future Internet, 9(4), 2017), El & Scopus Indexed

- Optimized Deep Neural Networks for Real-Time Object Classification on Embedded GPUs (Applied Sciences, 7(8), 2017), SCIE Indexed
- A General-Purpose Graphics Processing Unit (GPGPU)-Accelerated Robotic Controller Using a Low Power Mobile Platform

(Journal of Low Power Electronics and Applications, 7(2), 2017), Scopus Indexed

- GPU-only Unified ConvMM Layer for Neural Classifiers
 (In International Conference on Control, Decision and Information Technologies, April 2017, Spain)
- GPGPU Accelerated Deep Object Classification on a Heterogeneous Mobile Platform (MDPI Electronics, 5(4),2016), SCIE Indexed
- Comparison of GPGPU based Robotic Manipulator with other Embedded Controllers (In 13th International Conference on Development and Application Systems, May 2016, Romania)
- Gabor Filter based Image Representation for Object Classification

 (In International Conference on Control, Decision and Information Technologies, April 2016, Malta)

- Softwares/Languages
 - Pytorch, CUDA, Assembly Language, C/C++ Language, VHDL, MATLAB, Xilinx ISE, Keil, Proteus, Packet Tracer, WireShark, VMware Workstation, Microsoft Office, Internetwork Operating System for Cisco Devices, Windows and Linux Operating Systems.
- Hardwares
 - Nvidia GPUs (Quadro K2200, Nvidia Shield Tablet and Jetson Tx1 Board), AVR ATmega Family, Atmel based 8051 Family, Arduino Microcontrollers, FPGA (Sparten-3E kit), Cisco Routers and Switches.

TECHNICAL TRAININGS, WORKSHOPS AND SUMMER SCHOOLS

 Deep Learning or 	n-Chip Sept 20-22, 2017	Politecnico di Torino, Torino, Italy
 Biannual European - Latin American Summer School on Design, Test and Reliability May 30 - June 1, 2016 Politecnico di Torino, Torino, Italy 		
 CCNA (Training) 	July 2006- Sep 2006	University of Central Punjab, Lahore, Pakistan
MEMBERSHIPS		
 Member of Pakistan Engineering Council (Elect/24752). 		

• English (Fluent), Urdu (Mother Tongue).